VLSI SIGNAL PROCESSING

(Elective-II)

Course Code: 19EC2254

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Prerequisites: VLSI Design, Digital Signal Processing

Course outcomes: At the end of the course the student will be able to

CO1: Explain DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
CO2: Describe iteration bound, retiming techniques.
CO3: Summarize the folding and unfolding algorithms.
CO4: Outline the systolic architecture design.
CO5: Explain different convolution techniques and features of DSP Processors.

UNIT-I — 10 Lectures

DSP systems and algorithms

Introduction to DSP systems: Introduction, Overview of typical DSP Algorithms, Representation of DSP Algorithms: Block Diagrams, Signal-Flow Graph, Data-Flow Graph, Dependence Graph.

Pipelining and parallel processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing.

Learning outcomes: At the end of this unit, the student will be able to

1. Summarize the different representations of DSP Algorithms (L2)
2. Describe the pipelining for Low Power (L2)
3. Illustrate the parallel processing for Low Power (L3)

UNIT-II — 10 Lectures

Iteration Bound and Retiming

Introduction to Iteration bound, Data-Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound, Iteration Bound of Multirate Data-Flow Graphs. Introduction to retiming, Definitions and Properties, Solving Systems of Inequalities, Retiming Techniques.

Learning outcomes: At the end of this unit, the student will be able to

1. Derive Loop Bound and Iteration Bound (L6)
2. Formulate the iteration bound of multirate data-flow graphs (L6)
3. Describe Retiming Techniques (L2)

UNIT-III **10 Lectures**

Folding and Unfolding

Unfolding: Introduction, an Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming.

Folding: Introduction, Folding transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Learning outcomes: At the end of this unit, the student will be able to

1. Describe unfolding (L2)
2. Summarize folding and folding transformation (L2)
3. Analyze unfolding and folding concepts for register minimization (L4)

UNIT-IV **10 Lectures**

Systolic architecture design

Introduction, systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

Learning outcomes: At the end of this unit, the student will be able to

1. Discuss systolic array design methodology (L2)
2. Summarize FIR Systolic Arrays (L2)
3. Model 2D Systolic Array and Systolic design for space representations containing delays (L3)

UNIT-V **10 Lectures**

Convolution and Digital Signal Processors

Fast Convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution and Cyclic Convolution.

Programmable Digital Signal Processors: Introduction, Evolution of Programmable Digital Signal Processors, Features of DSP Processors.

Learning outcomes: At the end of this unit, the student will be able to

1. Apply fast convolution algorithms for signal processing applications (L3)
2. Summarize performance improvements and evolution of Programmable DSPs (L2)
3. Discuss features of DSP Processors (L2)

Text Books

Keshab K. Parhi, *VLSI Digital signal processing systems, design and implementation*', Wiley, Inter Science, 1999.

References

1. Mohammad Isamail and Terri Fiez, *Analog VLSI signal and information processing*, McGraw Hill, 1994
2. S.Y. Kung, H.J. White House, T. Kailath, *VLSI and Modern Signal Processing*, Prentice Hall, 1985.

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