MICROPROCESSORS & MICROCONTROLLERS

Course Code:20EC1120

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Prerequisites: Digital Logic Design

Course Outcomes: At the end of course the student will be able to
CO1**:** Describe the Architecture of 8086 Microprocessor (L2)
CO2: Illustrate programming skills in assembly language for 8086 Microprocessor (L3)
CO3: Outline the complete register set of ARM(L4)
CO4: Understand the Instruction set of ARM (L2)
CO5: Evaluate the optimizing of assembly code in ARM (L5)

UNIT-I 10 Lectures

8086 Architecture

Register organization of 8086, Architecture, Signal description of 8086, Physical memory organization, General bus operation, I/O addressing capability, Minimum Mode 8086 system and timings, Maximum mode 8086 system and timings, Addressing Modes of 8086.

Learning outcomes: At the end of this unit, the student will be able to

1. explain the functional description of 8086 (L2)
2. explain the different registers of 8086 microprocessor (L2)
3. discuss addressing modes of 8086 microprocessor (L2)

UNIT-II 12 Lectures

8086 Programming

Instruction set of 8086, Assembler Directives and Operators, Assembly language example programs, Stack Structure of 8086, Programmable peripheral interface 8255A, Need for DMA, 8257 DMA controller.

Learning outcomes: At the end of this unit the student will be able to

1. describe various instruction set of 8086 (L2)
2. demonstrate different assembly programs using instruction set of 8086 (L3)
3. discuss about programmable peripheral interface 8255 (L2)

UNIT-III 8 Lectures

ARM Processor Fundamentals

ARM core data flow model, Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table, Architecture revisions, Thumb Programmer's model, Thumb applications. (TEXT BOOK- 2 &3)

Learning outcomes: At the end of this unit the student will be able to

1. illustrate the ARM core dataflow model(L3)
2. explain the complete register set. (L2)
3. discuss Thumb programmer's model (L2)

UNIT-IV 10 Lectures

The ARM Instruction Set:

Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI), Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instructions, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP),Status register to general register transfer instructions, General register to status register transfer instructions. (TEXT BOOK-3)

Learning outcomes: At the end of this unit, the student will be able to

1. understand the branch instructions in ARM (L2)
2. explain the different Data processing instructions (L2)
3. discuss Swap memory and register instructions in ARM (L2)

UNIT-V 10 Lectures

Writing and Optimizing Assembly code:

Profiling and Cycle Counting: Instruction Scheduling, Scheduling of Load Instructions, Register Allocation: Allocating Variables to Register Numbers, Using More than 14 Local Variables: Making the Most of Available Registers, Conditional Execution:Looping Constructs: Decremented Counted Loops, Unrolled Counted Loops, Multiple Nested Loops, Other Counted Loops, Bit Manipulation: Fixed-Width Bit-Field Packing and Unpacking, Variable-Width Bitstream Packing, Variable-Width Bitstream Unpacking. (TEXT BOOK-2)

Learning outcomes: At the end of this unit the student will be able to

1. illustrate the different types of condition execution(L4)
2. explain about profiling and cycle counting (L3)
3. explain the Bit manipulation using fixed width and variable width (L3)

Text Books:

1. A.K.Ray and K.M.Bhurchandi, *Advanced Microprocessors and Peripherals*, 3rd Edition, TMH, 2012.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, *ARM System Developer's Guide: Designing and Optimizing System Software*, 1st Edition, Elseveir and Morgan Kaufmann Publishers, 2008.

3. Steve Furber, *ARM System-on-Chip Architecture*, 2nd edition, Addison-Wesley Professional, 2000.

References:

1. Gaonkar, Ramesh S. *Microprocessor Architecture, Programming and Applications with the 8085-8080a*. 6th Edition, Prentice Hall PTR, 2013.
2. Hall, Douglas V., Gregg division, and Computer Science Series. *Microprocessors and interfacing: programming and hardware*. 2nd Edition, McGraw-Hill, 2005.
3. Nilesh B.Bahadure, *Microprocessors: The 8086/8088, 80186/80286, 80386/80486 and the Pentium Family*., PHI., 2010.

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