RTL SIMULATION AND SYNTHESIS WITH PLDs

Course Code: 19EC2201

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Prerequisites: VLSI Design, Digital Logic Design

Course Outcomes: At the end of the course the student will be able to

CO1: Describe Finite State Machines and comprehend concepts of clock related issues.
CO2: Model digital circuits using Verilog and understand the concepts of analog and mixed signal Systems design using Verilog AMS.
CO3: Outline the concepts of different design flows in VLSI.
CO4: Illustrate different low power latches and Flip-flops.
CO5: Explain the concepts of IP cores and Prototyping.

UNIT-I — 10 Lectures

Design strategies

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

Learning outcomes: At the end of this unit, the student will be able to

1. Describe the Top down approach to design (L2)
2. Summarize the concepts of Finite state machines (L2)
3. Illustrate the concepts of clock related issues (L3)

UNIT-II — 10 Lectures

Modelling of digital circuits

Design entry by Verilog, Combinational and Sequential Logic Design : Multiplexer/ Demultiplexer, ALU, parity circuits, Flip-flops, Shift Registers, Counters, Finite State Machines, Sequence generator, Sequence detector, Verilog AMS.

Learning outcomes: At the end of this unit, the student will be able to

1. Model various combinational circuits using Verilog (L3)
2. Model various Sequential circuits using Verilog (L3)
3. Discuss the concepts of analog and mixed signal systems design using Verilog AMS (L2)

UNIT-III — 10 Lectures

Design methodologies

Programmable Logic Devices, FPGA, SoC, Introduction to ASIC Design Flow, Floor Planning, Placement, Clock tree synthesis, Routing, Physical verification.

Learning outcomes: At the end of this unit, the student will be able to

1. Describe the concepts of programmable Logic Devices (L2)
2. Demonstrate FPGA and ASIC design flows (L3)
3. Illustrate the concepts of CPLD and FPGA architectures (L3)

UNIT-IV — 10 Lectures

Low power Latches and Flip-flops

Introduction, Need for low power latches and flip-flops, Evolution of Latches and Flip-flops, Quality measures for latches and flip-flops, Design perspective.

Learning outcomes: At the end of this unit, the student will be able to

1. Demonstrate latches and flip-flop designs to improve performance (L3)
2. Interpret different low power design techniques (L2)
3. Illustrate the concepts of quality measures for latches and flip-flops (L3)

UNIT-V — 10 Lectures

IP and Prototyping

IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, use of external hard IP during prototyping.

Learning outcomes: At the end of this unit, the student will be able to

1. Describe the concepts of IP in various forms (L2)
2. Differentiate Soft IP and Hard IP (L2)
3. Illustrate the concepts of prototyping (L3)

Text Books

1. Richard S. Sandige, *Modern Digital Design*, MGH, International Editions,1990
2. T. R. Padmanabhan and B. F.V.G. Bala Tripura Sundari, *Design through Verilog HDL*, WSE, IEEE Press, 2004.
3. Zeidman, Bob. *Designing with FPGAS and CPLDS*. CRC Press, 2002.
4. KiatSeng Yeo, Samir S. Rofail, Wang-Ling Goh, *CMOS/Bi CMOS ULSI Low Voltage Low Power*, Pearson Education Asia 1st Indian reprint, 2002.
5. Doug Amos, Austin Lesea, Rene Richter, *FPGA based prototyping methodology manual*, Xilinx.

References

1. Palnitkar, Samir. *Verilog HDL: a guide to digital design and synthesis*. Pearson Education India, 2003.
2. Givone, Donald D. *Digital principles and design*. Palgrave Macmillan, 2003.
3. Roth, Charles H. *Digital systems design using VHDL*. Wadsworth Publ. Co., 1998.

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