DIGITAL LOGIC DESIGN
(Common to ECE, EEE, CSE, IT)

Course Code: 15EC1105

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Course Outcomes:

At the end of the course the student will be able to

CO 1 Convert a number from one number system to other Number system.

CO 2 Implement logic circuits using basic Logic gates or universal Logic gates and simplify logic expressions using basic theorems, K-map and Tabular method

CO 3 Explain the concept of Combinational logic design and Realize logic expressions using MUX, Decoder and PLDs.

CO 4 Illustrate the concept of sequential logic design, analyze the operation of flip-flop and design various types of sequential circuits.

CO 5 Differentiate Mealy & Moore models and Simplify & Design Sequential machines.

Unit-I (08 Lectures)

NUMBER SYSTEMS & CODES:

Introduction to number systems, Complement representation of negative numbers, binary arithmetic, binary codes, Error detecting & correcting codes.

UNIT-II (12 Lectures)

BOOLEAN ALGEBRA AND SWITCHING FUNCTION

Fundamental postulates of Boolean algebra, Basic theorems and properties, switching functions, Simplification of Boolean equations, Digital logic gates, properties of XOR gates, universal gates - NAND/

NOR realizations. K-map method, Prime implicants, don't care combinations, Minimal SOP and POS forms, Tabular Method, Prime –Implicant chart, simplification rules.

UNIT-III (10 Lectures)

COMBINATIONAL LOGIC DESIGN:

Adders, Subtractor, Multiplexer, De-Multiplexer, MUX Realization of switching functions, Encoder, Decoder, Parity bit generator, Code-converters, Basic PLD's-ROM, PROM, PLA, PAL Realizations.

UNIT-IV (12 Lectures)

SEQUENTIAL LOGIC DESIGN:

Classification of sequential circuits (Synchronous, Asynchronous, Pulse mode, Level mode with examples) Latches and Flip-flops-Triggering and excitation tables, registers, shift registers, Steps in synchronous sequential circuit design, synchronous counters, ripple counters, Design of modulo-N Ring & Shift counters, Serial binary adder.

UNIT-V (8 Lectures)

FINITE STATE MACHINES:

Finite state model- Basic Definition, Synthesis of Synchronous Sequential circuit – Sequence detector, Binary counter, Capabilities and limitations of FSM, Mealy and Moore models-minimization of completely specified sequential machines, Partition techniques, incompletely specified sequential machines using merger table and merger graphs.

TEXT BOOKS :

1. Morris Mano, *"Digital Design"* PHI, 3rd Edition, 2006.
2. Anand Kumar, *"Switching Theory and Logic Design"* PHI, 2008

REFERENCES :

1. Zvi Kohavi, "*Switching & Finite Automata theory*" TMH, 2nd Edition,
2. R.P. Jain. "*Modern Digital Electronics*", 4th ed., TMH, 2009.

3. John M. Yarbrough, "*Digital Logic Applications and Design*" Thomson Publications, 2006.
4. Charles H. Roth, "*Fundamentals of Logic Design*" Thomson Publications, 5th Edition, 2004.