DIGITAL DESIGN THROUGH VERILOG

(Open Elective)

COURSE CODE: 15EC1149

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COURSE OUTCOMES:

At the end of the course the student shall be able to

CO1: Describe the basic concepts of Verilog language.

CO2: Comprehend the structural procedures in Verilog language.

CO3: Illustrate tasks, functions and PLI.

CO4: Outline the concepts of verification.

CO5: Comprehend the concepts of System Verilog and Universal Verification Model (UVM).

UNIT-I (8 LECTURES)

INTRODUCTION TO VERILOG: Verilog as HDL, Levels of Design Description, Concurrency, Functional Verification, Module, Test Bench, Compiler Directives, Functions, Tasks, Language Constructs and Conventions: Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators.

UNIT-II (10 LECTURES)

STRUCTURAL PROCEDURES: Structural procedures: Initial, always, Initialization, blocking, non-blocking assignments, event based timing control, level sensitive based timing control, conditional statements, case, casex, casez statements. Loops: while, for, forever, repeat.

OPERATORS: operator types - binary, unary operators, logical, relational, equality, bitwise operators, Reduction, shift, concatenation, replication, conditional. Operator precedence.

UNIT III (12 LECTURES)

TASKS AND FUNCTIONS: Continuous assignments: Sequential, Parallel, nested blocks. Tasks, reentrant tasks, Functions, recursive functions. Def Parameter, conditional compilation-ifdef, Assignment delay, expressions.

PLI**:** uses, linking and invoking, Verilog coding style. FSM.

UNIT-IV (10 LECTURES)

VERIFICATION CONCEPTS: System Tasks and functions, File output- opening, writing, closing, Value change dump (.vcd), Random number generation, Directed testing, constrained random testing, parallel random testing , Black box testing, White box testing, Checkers, Score board, Functional coverage, Logs, Test bench block level, Integration level, Glue, Programming Language Interface (PLI).

UNIT-V (10 LECTURES)

INTRODUCTION TO SYSTEM VERILOG AND UVM: Predictors, Assertion base testing, Assertions- Concurrent, Immediate, Sequence- Edge, logical relationship, timing relationship, Simple action block, Timing windows, checker using parameters, Inter construct, or construct, Bus Functional Model (BFM), System Verilog Assertion(SVA) for FSM, Memory.

UVM: Basic test bench functionality, Protocol exceptions, errors, violations, Signals and command layers, functional layer, scenario layer, UVM test bench hierarchy

TEXT BOOKS:

1.Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall PTR, 2003.

2. Srikanth Vijayaraghavan, Meyyappan Ramanathan, "A Practical Guide for System Verilog Assertions", Springer, 2005.

3. Cook Book Mentor Graphics, http://verificationacademy.com.

REFERENCES:

1.T.R. Padmanabhan and B. Bala Tripura Sundari, "Design through Verilog HDL'', WSE, 2004 IEEE Press.

2. J. Bhaskar, "A Verilog Primier", BSP, 2003.

3. Michael D. Ciletti, "Advanced Digital Design with Verilog HDL", Phi,2005.

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